State-Of-The-Art Approach To Mitigate Risk Of Die Crack With Substrate Co-Planarity Issue

Cham Hooi Ying[1*], Ooi Jen Wai[2], Tan Thian Yik[2], Tan Yin Heng[1], Ng Kok Aun[1]

[1]Quality Assurance Department, ASE Electronics (M) Sdn Bhd. Bayan Lepas FIZ, Penang, Malaysia

[2]FOL Engineering Department, ASE Electronics (M) Sdn Bhd. Bayan Lepas FIZ, Penang, Malaysia

ABSTRACT

- Miniaturization drives DAF adoption, replacing epoxy for better IC packaging.
- Delamination/voids cause die cracks in DAF due to substrate topography.
- Optimizing die attach parameters reduces voids and enhances IC packaging reliability.

INTRODUCTION

- Die Attach process is a crucial step in the semiconductor industry where the chip (die) is attached to a substrate using adhesive material, Die Attach Film (DAF), a thin adhesive film activated by heat and pressure.
- Processing DAF material presents challenges, with DAF void being a major concern that makes packages more prone to delamination and cracking.
- The substrate's design layout can induce various stress distributions that directly affect the IC chip during assembly processes, leading to die crack damage.
- The primary objective of this research is to investigate the causes and impact of DAF void in BGA packages.
- This study aims to improve die attach parameters to reduce void formation.

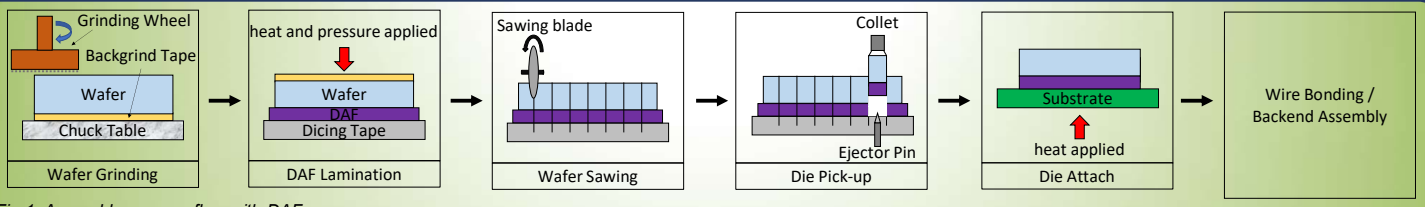

Fig 1. Assembly process flow with DAF.

METHODS

- Voids and die cracks inspection using SAT (Scanning Acoustic Tomography).
- Surface topology of a substrate is investigated using 3D measuring laser microscope.
- Die attach parameters are optimized using Design of Experiment (DOE) approach.

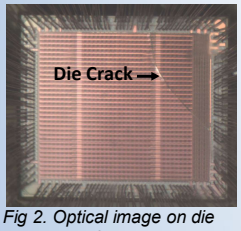

Fig 2. Optical image on die crack unit after decapsulation.

Leg	Bond Delay (ms)	Bond Temp (°C)	Die Crack Screening Post DA	Post Mold	Post Saw	Total Die Crack (%)	Average Void (%)
1	Low (300)	Low (100)	0/28	2/28	2/28	7.14	10.70
2	High (500)	Low (100)	0/28	1/28	1/28	3.57	4.15
3	Low (300)	High (140)	0/28	0/28	0/28	0	1.52
4	High (500)	High (140)	0/28	0/28	0/28	0	0.70

RESULTS AND DISCUSSION

A. Die Crack Characteristic

- DAF voids were observed in the area where the crack propagated, particularly in the uneven solder mask area with lower substrate thickness, indicating a correlation between void formation and die crack initiation.
- Cross-sectional analysis showed that voids at the substrate-DAF interface coincided with the area of die cracks, indicating a correlation between voids and die cracks.

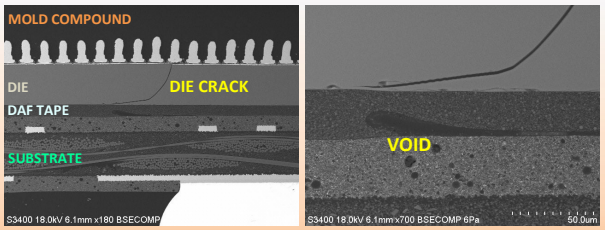

Fig 3. Cross-section image of die crack unit.

B. Correlation Between Substrate And Void

- Examination of the substrate's surface topology using a 3D measuring laser microscope revealed uneven die attach pad (DAP) surface, with the die crack area exhibiting the lowest height.
- The substrate surface planarity is suspected to be the primary contributor to the formation of DAF voids, which in turn led to die cracks.

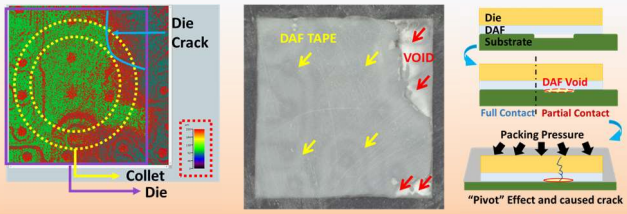

Fig 4. Die crack mechanism.

C. Die Attach Parameter

- DOE study shows that higher bonding temperature (140°C) and longer bond delay (500ms) reduced DAF void percentage, indicating the significance of these parameters in void reduction.
- The additional heat helps melt the DAF and fill uneven substrate planarity, while increased bond delay allows for better heat absorption and adhesion of the DAF.

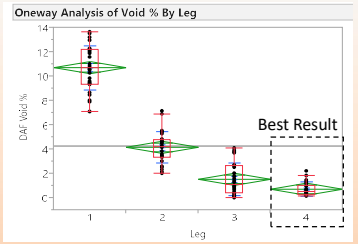

Fig 5. DOE parameter settings in response to DAF void percentage.

CONCLUSIONS

- This study establishes a correlation between substrate co-planarity, DAF void formation, and die cracks in BGA packages.
- Optimizing die attach parameters, can effectively reduce DAF voids, resulting in enhanced reliability and performance of the package.

ACKNOWLEDGMENT

- The authors acknowledge the technical and financial supports from Advance Semiconductor Engineering (ASE) Malaysia.